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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/437,580	11/09/1999	ALEXANDER G. MACINNIS	36101/SAH/B6	8182

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EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 04/06/2004

28

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/437,580	MACINNIS ET AL.	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,19 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,19 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 01/22/2004 is entered. The arguments have been fully considered but they are not persuasive. The rejections of claims 1-15, 19, 21-25 are maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15, 19 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tateyama "previously cited" (US 5,515,077) in view of Sokawa et al "previously cited" (US 6,353,460).

1. As to claim 1, Tateyama teaches the method of horizontally scrolling a display window to the left comprising the steps of

receiving a data packet (Y0 Y1 U0 V0) (figure 28) that includes a field for a blank start pixel value (Y0 U0 V0), which indicates a number of pixels to be blanked out;

blanking out one or more pixels (Y0 U0 V0) at a beginning of a portion of graphics data in accordance with the blank start pixel value;

displaying the graphics data starting at a first non-blanked out pixel in the portion of the graphics data aligned with the start address (see figure 22, column 9, lines 1-12).

Tateyama fails to teach "placing a read pointer at a location after one or more pixel, displaying the graphics data starting at the read pointer at a first non-blanked out

pixel in the portion of the graphics data aligned with the start address." However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Sokawa teaches a header data packet comprising the RGB signal data (col. 16, line 51), the image data unit of one pixel is 16 bits (col. 22, line 14), the head of the image data unit VSj, and the tail of the image data unit of the former half VSi (fig. 22, col. 28, lines 25-27).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Tateyama's read timing providing the read pointer, in view of the teaching in the Sokawa's reference because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 2, Tateyama teaches converting the graphics data into a common format (see column 10, line 35).

As to claims 3, 5, 6, Tateyama teaches blanking out four-bit color data (0,1,0,0) (see column 9, line 1).

As to claim 4, Tateyama teaches the common format is selected from the group of YUV and RGB formats (see figures 13 and 14, column 3, lines 60-61).

2. *As to claim 7*, Tateyama teaches the method of horizontally scrolling a display window to the right comprising the steps of

receiving a data packet (Y0 Y1 U0 V0) (figure 28) that includes a field for a blank start pixel value (Y0 U0 V0), which indicates a number of pixels to be blanked out;

blanking out one or more pixels (Y0 U0 V0) at a beginning of a portion of graphics data in accordance with the blank start pixel value;

displaying the graphics data starting at a first non-blanked out pixel in the portion of the graphics data aligned with the start address (see figure 23, column 9, lines 13-20).

Tateyama fails to teach "placing a read pointer at a location after one or more pixel, displaying the graphics data starting at the read pointer at a first non-blanked out pixel in the portion of the graphics data aligned with the start address." However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Sokawa teaches a header data packet comprising the RGB signal data (col. 16, line 51), the image data unit of one pixel is 16 bits (col. 22, line 14), the head of the image data unit VSj, and the tail of the image data unit of the former half VSi (fig. 22, col. 28, lines 25-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Tateyama's read timing providing the read pointer, in view of the teaching in the Sokawa's reference because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 8, Tateyama teaches converting the graphics data into a common format (see column 10, line 35).

As to claims 9, 11, 12, Tateyama teaches blanking out four-bit color data (0,1,0,0) (see column 9, line 1).

As to claim 10, Tateyama teaches the common format is selected from the group of YUV and RGB formats (see figures 13 and 14, column 3, lines 60-61).

3. *As to claim 13*, Tateyama teaches a graphic display system which includes a display engine "background Processing unit", a window controller "scroll box, superimpose box", a data packet (figure 28), a direct memory access "K-RAM" (figure 30, column 9, line 53 through column 10, line 14).

Tateyama fails to teach a read pointer for scrolling image. However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a

first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Sokawa teaches a header data packet comprising the RGB signal data (col. 16, line 51), the image data unit of one pixel is 16 bits (col. 22, line 14), the head of the image data unit VSj, and the tail of the image data unit of the former half VSi (fig. 22, col. 28, lines 25-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Tateyama's read timing providing the read pointer, in view of the teaching in the Sokawa's reference because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 14, Tateyama teaches the display engine "background processing unit" (figure 30, column 4, lines 40-41). Sokawa et al teaches displaying the graphics data starting at the read pointer (P_R) with the offset start time when horizontal scrolling will be carried out (see figure 12A to 12B, column 22, lines 23-30). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Tateyama's read timing providing the read pointer, in view of the teaching in the Sokawa's reference because this would minimize the total size circuit configuration

which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 15, Tateyama teaches a direct memory access "K-RAM" (column 4, lines 40-41).

As to claim 19, Tateyama teaches the first non-blanked out pixel is a first pixel is displayed (see figure 7, column 2, line 36-37).

4. *As to claim 21*, Tateyama teaches a graphic display system which includes a display engine "background Processing unit", a window controller "scroll box, superimpose box", a data packet (figure 28), a direct memory access "K-RAM" (figure 30, column 9, line 53 through column 10, line 14).

Tateyama fails to teach a read pointer for scrolling image. However, Sokawa et al teaches displaying the graphics data starting at a read pointer (Pr) is initially placed on a first portion of the raw graphic data (the first input buffer portion) aligned with a start address (0) (see figure 12B, column 22, lines 27-31); in order to realize the moving image real time processing system (column 25, lines 56-59), the read pointer (Pr) is moved to the right to a second portion of the raw graphics data (a second input buffer portion) aligned with a new start address (M/2) (figure 12D, column 22, lines 51-58).

Sokawa teaches a header data packet comprising the RGB signal data (col. 16, line 51), the image data unit of one pixel is 16 bits (col. 22, line 14), the head of the image data unit VSj, and the tail of the image data unit of the former half VSi (fig. 22, col. 28, lines 25-27).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Tateyama's read timing providing the read pointer, in view of the teaching in the Sokawa's reference because this would minimize the total size circuit configuration which can be used for a variety of applications, improve the quality of the image being displayed, while fabricating a video signal processing device at low cost (see column 9, lines 10-20 of Sokawa et al).

As to claim 22, Tateyama teaches a direct memory access "K-RAM" (column 4, lines 40-41).

As to claim 23, Tateyama teaches the first non-blanked out pixel is a first pixel is displayed (see figure 7, column 2, line 36-37).

As to claim 24, Sokawa et al teaches the display engine "background Processing unit" for blanking out one or more pixels from a second input buffer portion by selectively placing the read pointer (Pr) (figure 12D, column 22, lines 51-58).

As to claim 25, Sokawa teaches a header data packet comprising the RGB signal data (col. 16, line 51), the image data unit of one pixel is 16 bits (col. 22, line 14), the head of the image data unit VSj, and the tail of the image data unit of the former half VSi (fig. 22, col. 28, lines 25-27).

Response to Arguments

5. Applicant's arguments filed 01/22/2004 have been fully considered but they are not persuasive.

Applicant states during the interview filed on 01/16/2004, an agreement was reached that claims 1-15, 19 and 21-25 as amended by the proposed claim

amendments (submitted on January 15, 2004) and as required by the required by the Examiner during the telephone interview, overcome the rejection over Tateyama and Sokawa . In response, Examiner disagrees because Applicant requested for a telephone interview on January 15, 2004, Examiner did not require the telephone interview on January 15, 2004.

In response to applicant's argument that claims 1 and 7 recites "a head data packet that includes a field for a blank start pixel value, which indicates a number of pixels to be blanked out." This argument is not persuasive because Teteyama teaches the claimed limitation "a head data packet" (see fig. 28).

Sakawa teaches Referring to fig. 7 and fig. 22 input section 2040 receiving is configured to be able to receive up to two sets of 16 bit digital video signals (col. 18, lines 64-66). The scan video processor SVP2014 includes three-layer structure composed of a data input register DIR 2016, a processing portion 2018, and a data output register DOR 2020 (col. 19, lines 58-61). The head of the image data unit is the later half VSj (col. 28, lines 25-26). Once the first input buffer portion is filled with the input image data, the write pointer Pw points to the head address of the second (right) input buffer portion which is vacant (col. 22, lines 23-25). That means blanking out one or more pixels start at the address (0) to the address where the read pointer P_R points (see fig. 12C). A read pointer P_R points to the head address of the first input buffer portion, starting the read of the input image data from the first input buffer portion (fig. 12B, col. 22, lines 27-31).

These arguments are not persuasive because packet header defines in Microsoft Computer Dictionary, fourth edition, the portion of a data packet that precedes the body (data). The header contain data such as source and destination addresses, and control and timing information, that is needed for successful transmission. Therefore, the combined teaching of Tateyama and Sokawa meet the claimed limitation "the header data packet."

For these reasons, the rejections based on Tateyama and Sokawa et al have been maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
March 26, 2004

XIAO WU
PRIMARY EXAMINER